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METHOD AND APPARATUS FOR TESTING DRAM MEMORY CHIPS IN MULTICHIP MEMORY MODULES

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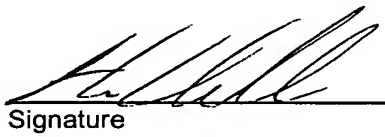

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METHOD AND APPARATUS FOR TESTING DRAM MEMORY CHIPS IN MULTICHIP MEMORY MODULES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number 103 16 931.8, filed April 12, 2003. This related patent application is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The invention relates to a method and an apparatus for testing DRAM memory chips in multichip memory modules.

Description of the Related Art

[0003] Multichip memory modules, which combine a DRAM memory chip (volatile memory) and a flash chip (nonvolatile memory) in one housing, are increasingly gaining market share for memory components for apparatuses for mobile applications, e.g., mobile telephones or notebooks. While the flash chip stores programs and data which have to be retained even when the operating voltage is switched off, the DRAM memory chip is used to ensure fast access to data and program parts in an operative operating mode of the application apparatus.

[0004] An emerging trend is production of the multichip memory modules in the context of so-called Known-Good-Die (KGD) business models. This means that it is ensured that the unpackaged memory chip satisfies the same quality standard as the packaged memory chip. In the context of the KGD business models, DRAM memory chips and flash chips that have been tested at the wafer level are packaged in a multichip memory module and supplied, if appropriate, after a short component test. The question of an expected early failure rate of the multichip memory modules arises in this case. Manufacturers of flash chips solve this problem partly by means

of a pure thermal stress of the wafers without an additional electrical stress, as a result of which an early failure of the flash chips is accelerated.

[0005] A customary way of lowering the early failure rate of DRAM memory chips consists of a burn-in lasting a number of hours (e.g., 2 to 20 hours), the duration of the operation depending on the state of the technology, the memory size and the production quality sought. In this case, each individual DRAM memory chip is exposed to continuous electrical stress at an elevated temperature. A simulation of this method at the wafer level is associated with considerable costs and technical problems, such as, for example, the requirement for simultaneous contact-connection of all the chips on the wafer. It is generally the case, therefore, that, under certain circumstances, greatly shortened test times are employed and, as a result thereof, a relatively high early failure rate of the DRAM memory chips is accepted, in a disadvantageous manner.

[0006] Typical applications of DRAM memory chips relate for example to graphical applications of the apparatuses mentioned, such as, by way of example, an image memory for the display of the mobile telephone. In these applications, a few pixel defects do not result in critical impairment of the functionality of the application. However, DRAM memory chips are also used as buffer memories for program parts and data, in the case of which a failure of memory cells of the DRAM memory chips can have an extremely disadvantageous effect. As a result, a high early failure rate can considerably impair the reliability of the DRAM memory chips and thus represent a non-negligible disadvantage.

[0007] Consequently, the object of the present invention is to provide a method and an apparatus which can be used to increase the reliability of DRAM memory chips in multichip memory modules, particularly for multichip memory modules being incorporated in apparatuses for mobile applications.

SUMMARY OF THE INVENTION

[0008] One embodiment of the invention provides a method for testing memory cells of a DRAM memory chip being arranged together with a nonvolatile memory chip in

a multichip memory module. The multichip memory module may be incorporated in an application apparatus, in particular in a mobile telephone or in a notebook. The DRAM memory chip is subjected to a self-test, during which a functionality of the memory cells is checked, in a time in which the memory cells of the DRAM memory chip are not accessed in an operative operating mode of the application apparatus.

[0009] Consequently, the method according to one embodiment of the invention advantageously provides an additional operating mode of the DRAM memory chip, the additional operating mode carrying out a self-test of the DRAM memory chip in phases in which the apparatus is not used for the mobile application (e.g., a charging operation for a rechargeable battery or a relatively long standby time of the mobile telephone or notebook). In this case, it is generally possible to have recourse to integrated circuits which are used for the regular testing of the DRAM memory chip in the fabrication process.

[0010] In one embodiment, the method provides for a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip to be connected, in order to store defect addresses of defective memory cells of the DRAM memory chip in the nonvolatile memory chip. This advantageously supports identification of the defective memory cells in the DRAM memory chip.

[0011] Another embodiment of the method provides for a self-test control device arranged in the DRAM memory chip to be used to select addresses of the DRAM memory chip, and for a central processing unit to select addresses of the nonvolatile memory chip. This advantageously supports the fact that the DRAM memory chip autonomously addresses an internal memory cell structure with the aid of the self-test control device. As a result, the central processing unit is relieved of the addressing of the memory cells of the DRAM memory chip, or need not be informed about the internal memory cell structure of the DRAM memory chip.

[0012] The method may further provide for defective memory cells in the DRAM memory chip that have been identified by means of the self-test to be replaced by redundant memory cells. This advantageously makes it possible to use redundant memory cells which are produced as standard in the course of the process for

fabricating the DRAM memory chip, the addresses of the redundant memory cells being read with the aid of soft fuses when the DRAM memory chip is started up. It is thus advantageously possible also to use redundant memory cells present on the DRAM memory chip after the regular fabrication process for the purpose of repairing the defective memory cells.

[0013] A further embodiment of the method provides for the self-test to be carried out during a rechargeable battery charging operation and/or during a standby time of the application apparatus. This means that times in which the application apparatus is not used operatively can advantageously be used for testing the DRAM memory chip.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0015] Figure 1 is a basic block circuit diagram illustrating a multichip memory module with an exemplary embodiment of a testing apparatus according to one embodiment of the invention; and

[0016] Figure 2 is a basic block diagram illustrating an application apparatus in which a testing apparatus according to one embodiment of the invention is utilized.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Figure 1 is a basic block circuit diagram illustrating a multichip memory module with an exemplary embodiment of a testing apparatus according to one embodiment of the invention. The illustration shows a simplified block diagram of a multichip memory module 1 having a DRAM memory chip 2 and a nonvolatile

memory chip 3 having terminals which are relevant to the apparatus according to one embodiment of the invention. Further functional terminals are possible, but may have no influence on the presented principle and are therefore not illustrated. The block diagram is extended by elements of a test device with a self-test control device 5. Two operating modes can be distinguished in the multichip memory module 1:

- functional mode (the elements depicted by broken lines are ineffectual in this mode)
- self-test mode (elements depicted by broken lines are activated)

[0018] By means of the self-test control device 5, the method according to one embodiment of the invention can be initiated by a central processing unit 11 (not illustrated in Figure 1; shown in Figure 2) arranged outside the multichip memory module 1.

[0019] As known from conventional memory chips, the terminals of the multichip memory module 1, comprising the DRAM memory chip 2 and the nonvolatile memory chip 3, can be classified into three groups:

- control terminals (these are generally inputs, a so-called ready/busy output often being provided in the case of the nonvolatile memory chip 3, said ready/busy output indicating an availability of the nonvolatile memory chip 3),
- address terminals (inputs) which are partly used jointly in the multichip memory module 1 by the DRAM memory chip 2 and by the nonvolatile memory chip 3, and
- data terminals (bidirectional) which are generally used jointly in the multichip memory module 1 by the DRAM memory chip 2 and by the nonvolatile memory chip 3.

[0020] Table 1 below shows a list of terminals at the DRAM memory chip 2 and also terminals at the nonvolatile memory chip 3 which are relevant to the method according to one embodiment of the invention.

Pin/pin group	Functional mode	Self-test mode
F-RST/STI	Flash Reset (input)	Clock for self-test circuit, if appropriate interruption/termination of the self-test (input)
F-CS	Flash Chip Select (input)	ineffectual
F-OE	Flash Output Enable(input)	ineffectual
F-WE	Flash Write Enable (input)	ineffectual
D-CS	DRAM-Chip Select (input)	ineffectual
D-OE	DRAM-Output enable (input)	ineffectual
D-WE	DRAM Write Enable (input)	ineffectual
F_RDY/STO	Flash Ready/Busy (output)	Self-test running/ended/-next flash address required (output)
A[0:n]	Common address bus flash/DRAM (inputs)	Address bus flash (inputs) ineffectual for DRAM addresses
DQ[O:m]	Common data bus flash/DRAM (bidirectional)	Switched off (Hi-Z). If solution No. 1 in Tab. 2 used: outputting of the DA

Table 1

[0021] Table 1 reveals that the listed terminals at the DRAM memory chip 2 and at the nonvolatile memory chip 3 have a different functionality in a functional mode and a self-test mode of the multichip memory module 1. In the self-test mode, which may take place during a rechargeable battery charging operation of the apparatus in which the multichip memory module 1 is incorporated, the self-test is triggered by a corresponding mode register command by the central processing unit 11.

[0022] From this point in time, the self-test control device 5 controls the terminals F-CS (Flash Chip Select), F-OE (Flash Output Enable), F-WE (Flash Write Enable) at the nonvolatile memory chip 3 and also the terminals D-CS, D-OE and D-WE at the DRAM memory chip 2. The driving of the terminals F-CS, F-OE and F-WE requires additional bonding connections within the multichip memory module 1. After the self-test has been triggered with the aid of the self-test control device 5, the six terminals mentioned can no longer be driven from outside the multichip memory module 1 by means of an electronic switch device, for example a driver stage (not illustrated in

Figure 1), being switched off. Furthermore, an internal data bus F-DQ at the nonvolatile memory chip 3 is connected to a data bus T-DQ at the DRAM memory chip 2 and external terminals DQ [0:m] are switched to high impedance with the aid of a switch device 7 and switched off outside the multichip memory module 1.

[0023] The self-test control device 5 also controls addresses D-A at the DRAM memory chip 2 in the course of the method according to one embodiment of the invention. Moreover, addresses F-A at the nonvolatile memory chip 3 are furthermore selected by the central processing unit 11. The connecting lines to the self-test control device 5, illustrated by broken lines in Figure 1, indicate that these are operated in the self-test mode. The illustration of a voltage or current supply has been dispensed with in the figure for reasons of clarity. Terminals at the multichip memory module 1 which are passed toward the outside are illustrated in hatched fashion.

[0024] For the test method according to one embodiment of the invention, the DRAM memory chip 2 is internally divided into N test areas, for example, banks (not illustrated). Each of these test areas is allocated one or more addresses of the nonvolatile memory module 3 for storing information about effective memory cells 4. Said information may comprise, for example, a defect address and/or a soft fuse setting of the DRAM memory chip 2.

[0025] A chronological sequence of the method according to one embodiment of the invention is described as follows. A clock signal is applied to the terminal STI by the central processing unit 11. As soon as the clock signal fails to appear at the terminal STI for longer than one to two periods, the multichip memory module 1 leaves the functional mode, as a result of which the terminal STO is switched to high level, which signals to the central processing unit 11 that the self-test control device 5 is active. At the same time, the central processing unit 11 selects that address of the nonvolatile memory chip 3 in which, if appropriate, test results with respect to the first test area can be stored.

[0026] The self-test control device 5 thereupon carries out, via an address decoding circuit 6a, 6b, an addressing of the memory cells 4 of the DRAM memory chip 2 and

carries out, with the memory cells 4, test algorithms together with test settings of internal supply voltages and times. The test algorithms in the self-test control device 5 may be configured as traditional BIST (Built-In Self-Test) implementation. The writing of the data is effected via the data bus D-DQ of the DRAM memory chip 2 and also via a data bus F-DQ of the nonvolatile memory chip 3 and is controlled by the self-test control device 5. A low pulse lasting one to two clock cycles at the terminal STO causes the central processing unit 11 to apply an address for the next test area of the DRAM memory chip 2. After N low pulses at the terminal STO, the entire test operation is ended.

[0027] Depending on a chosen treatment of the detected defect address (see Table 2), further operations controlled by the self-test control device 5 may be effected in the DRAM chip 2 (e.g., setting of soft fuses). A final low pulse at the terminal STO signals to the central processing unit 11 that the self-test has ended and that the multichip memory module 1 has been switched back into the functional mode.

[0028] Since, after the supply voltage of the apparatus has been switched off, the multichip memory module 1 is not able to store the defect-related information (e.g., defective and repaired memory cells, unused defect addresses, etc.) of preceding self-tests, the multichip memory module 1 may be switched into the self-test mode each time the multichip memory module 1 is started up, in order to reestablish the defect-related information of preceding tests in the DRAM memory chip 2. A further mode register command may be used for this purpose to cause the self-test control device 5 to carry out only a very short initial self-test or no initial self-test.

[0029] Table 2 illustrates the way in which the method according to one embodiment of the invention enables the treatment of defective memory cells 4 identified in the self-test.

No.	Description	DRAM	Central processing unit
1	Masking out of DA	No additional measures	The DA are read from the flash by the central processing unit and not used.
2		The DA are read from the flash during start-up by the test circuit. A corresponding DA is skipped by the address decoding circuit.	No additional measures
3	Use of redundant elements of the DRAM	1-2 (tested) redundant word lines are kept per DRAM unit (e.g. bank), and are read, if appropriate, during start-up (depending on the flash content) by soft fuse.	No additional measures

Table 2

DA ... defect address

[0030] Table 2 reveals that, in principle, there are two different possibilities for treatment of the defective memory cells 4 identified in the self-test. On the one hand, defective addresses that have been identified can be masked out, i.e., excluded from use (No. 1, No. 2); on the other hand, the defective addresses may be replaced by redundant memory elements 4 (No. 3).

[0031] Two different possibilities are conceivable when masking out the defective addresses. On the one hand, the central processing unit 11 may read out the defective addresses stored in the nonvolatile memory chip 3, so that the defective addresses are no longer used in the operative mode of the multichip memory module 1. On the other hand, the treatment of the defective addresses may be effected directly in the DRAM memory chip 2, in that the defective addresses are read from the nonvolatile memory chip 3 by the self-test control device 5 during start-up. An addressed defective address is skipped by the address decoding circuit 6a, 6b. As a result, it is thus possible to leave the treatment of the defective addresses completely in the DRAM memory chip 2, which advantageously entails increased customer-

friendliness and user-friendliness that may reduce the available storage density at the DRAM memory chip 2.

[0032] The second fundamental possibility for the treatment of the defective addresses consists of using redundant elements of the DRAM memory chip 2. For this purpose, one or two tested redundant word lines or memory cells are made available per unit (e.g., bank) of the DRAM memory chip, and their addresses are read, if appropriate, during the start-up of the multichip memory module 1, depending on the content of the nonvolatile memory chip 3, by soft fuse. In this way, it is beneficially possible to repair individual defective memory cells after a repair process in production by reading or setting the soft fuse.

[0033] When using the redundant elements, it must generally be taken into account that the DRAM memory chip 2 has already undergone the test that is customary for wafers at this point in time. This generally includes a repair, i.e., a permanent replacement of the defective memory cell by redundant elements. Consequently, the number of defective cells still found by means of the self-test described above is correspondingly small and typically amounts approximately to one to two cells or addresses per memory bank. Like the soft fuses, the redundant elements (additional word lines and columns) presented under No. 3 in Table 2 are generally present in multiples on the DRAM memory chip 2.

[0034] To summarize, the method according to one embodiment of the invention can thus be classified according to the following criteria:

a) scope of the tasks which are swapped to the central processing unit 11 during the self-test, and

b) treatment of the effective memory cells 4 in the DRAM memory chip 2 by means of a self-test logic in the DRAM memory chip 2 or by means of the central processing unit 11.

[0035] The solution according to embodiments the invention is advantageously applied such that the circuit logic required for testing the DRAM memory chip 2 is not

accessible to a user. Consequently, the solution precludes configurations in which the central processing unit 11 stimulates the multichip memory module 1 for testing. The solution according to the invention advantageously provides the use of a BIST circuit on the DRAM memory chip 2. Such circuits are used currently by many manufacturers of DRAM memory chips 2 for the regular testing of DRAM wafers and components. This circuit may additionally have recourse to further test circuits present on the DRAM memory chip 2, for example, for adjusting internal supply voltages and timings. The method according to embodiments of the invention thus advantageously permits a reusability of test structures already present.

[0036] A particularly high flexibility of the method according to embodiments of the invention is provided by virtue of the fact that the central processing unit 11 may be practically not required. The central processing unit merely has to initiate, and if appropriate, terminate or interrupt, the self-test. This is generally associated with an increased outlay in terms of hardware (chip area, design, scope).

[0037] The method according to one embodiment of the invention takes account of two existing typical features of multichip memory modules 1 which are incorporated in applications such as, for example, mobile telephones and notebooks:

- frequent change between operative operating mode and charging mode,
- an integrated nonvolatile flash memory for storing and reading out data.

[0038] Furthermore, the method according to one embodiment of the invention is based on the assumption that the multichip memory module 1 is driven by a central processing unit 11 (processor or controller) on a circuit board of the apparatus for the mobile application.

[0039] A time schedule which can be used to control a specific number of self-tests according to the invention may be stored in the nonvolatile memory chip 3. As a result, it is possible, in an advantageous manner, to permanently deactivate the self-test after a certain time. This is justified with regard to early failures of the memory cells which are already largely precluded at this point in time.

[0040] An apparatus according to one embodiment of the invention may provide the self-test control device 5 on the nonvolatile memory chip 3 as well, thereby advantageously increasing the available chip area at the DRAM memory chip 2.

[0041] Figure 2 shows a basic block diagram illustrating an application apparatus in which a testing apparatus according to one embodiment of the invention is utilized. An application apparatus 8 (for example a mobile telephone or a notebook) comprises the multichip memory module 1, a rechargeable battery 9 and an identifying device 10. The rechargeable battery 9 is connected to the multichip memory module 1 and supplies the latter with a suitable operating voltage. The rechargeable battery 9 is furthermore connected to the identifying device 10, which can identify a charging state/operation of the rechargeable battery 9 or a change of rechargeable battery or a relatively long standby time of the application apparatus 8. A central processing unit 11 is connected to the identifying device 10 and to the multichip memory module 1. With the aid of the identifying device 10, the method according to one embodiment of the invention may be initiated by means of the central processing unit. The rechargeable battery 9 generally remains in the apparatus 8 during the charging operation, so that the time required for the method according to one embodiment of the invention expediently does not shorten the operative operating time of the apparatus.

[0042] The method according to one embodiment of the invention may furthermore be used advantageously in those cases in which the rechargeable batteries used in the apparatus 8 are charged exclusively externally. In this case, the self-test may be executed, for example, each time the rechargeable batteries are changed or after the apparatus 8 has been switched off, in accordance with the time schedule stored in the nonvolatile memory chip 3.

[0043] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.